In the Claims

1. (presently amended) A floating gate memory device comprising a plurality of transistor gate layers, comprising:

a transistor floating gate layer;

a first silicon dioxide layer overlying said floating gate;

a silicon nitride layer overlying said first silicon dioxide layer, said silicon nitride layer having a lower portion and an upper portion, wherein the upper portion is exposed;

a concentration of silicon atoms in said lower portion;

a concentration of silicon atoms in said upper portion,

wherein said silicon atom concentration in said lower portion of said nitride layer is less than said silicon atom concentration in said upper portion of said nitride layer, and said silicon concentration generally stays the same or increases throughout said nitride layer from said lower portion to said upper portion.

2. (presently amended) An in-process floating gate memory device comprising a transistor gate stack assembly, said assembly comprising:

a blanket unetched conductive floating gate layer;

a silicon dioxide layer overlying said unetched floating gate layer;

a silicon nitride layer overlying said silicon dioxide layer; and

an exposed oxidizable layer consisting essentially of a material selected from the group consisting of polycrystalline silicon and amorphous silicon,

wherein said gate stack assembly of said in-process floating gate memory device is absent any portion of a conductive control gate layer.

3. (presently amended) An in-process semiconductor device, comprising:

a semiconductor wafer substrate assembly comprising a semiconductor wafer, a gate oxide layer, and a conductive floating gate layer;

a silicon nitride layer overlying said floating gate layer, said silicon nitride layer having lower surface, an upper surface which is exposed, and an enhanced concentration of silicon atoms, wherein said enhanced concentration of silicon atoms has a gradation which stays the same or increases throughout said silicon nitride layer from said lower surface to said upper surface.

4. (original) The in-process semiconductor device of claim 3, wherein said in-process semiconductor device is absent any conductive control gate layer.

5. (original) The in-process semiconductor device of claim 3 further comprising a lower portion of said silicon nitride layer and an upper portion of said silicon nitride layer, wherein said upper portion of said silicon nitride layer comprises all of said silicon nitride layer except said lower portion and said concentration of silicon atoms remains the same throughout said lower portion of said silicon nitride layer and said concentration of silicon atoms increases throughout said upper portion of said silicon nitride layer.

6. (original) The in-process semiconductor device of claim 3 further comprising a lower portion of said silicon nitride layer and an upper portion of said silicon nitride layer, wherein said upper portion of said silicon nitride layer comprises all of said silicon nitride layer except said lower portion and said concentration of silicon atoms remains the same throughout said lower portion of said silicon nitride layer and remains the same throughout said upper portion of said silicon nitride layer, and said concentration of said silicon atoms in said upper portion is higher than said concentration of said silicon atoms is said lower portion.